(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 September 2003 (25.09.2003)

PCT

(10) International Publication Number
WO 2003/079172 A3

(51) International Patent Classification[7]: G06F 1/32

(21) International Application Number: PCT/US2003/004519

(22) International Filing Date: 14 February 2003 (14.02.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/095,864 11 March 2002 (11.03.2002) US

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(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

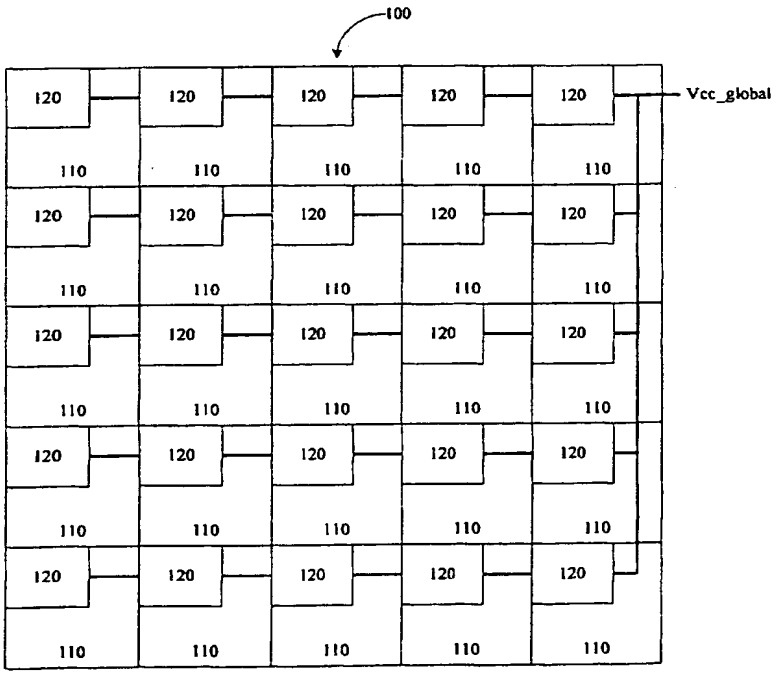
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report: 5 August 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A POWER-DOWN SCHEME FOR AN INTEGRATED CIRCUIT



(57) Abstract: According to one embodiment, an integrated circuit (100) is disclosed. The integrated circuit includes a plurality of circuit blocks (110). Each circuit block includes a voltage differentiator (120) that generates a local supply for the circuit block.

WO 2003/079172 A3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/04519

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/054760 A1 (ASHIGA KOICHI ET AL) 27 December 2001 (2001-12-27) paragraphs '0001!,'0002!,'0024!-'0028!,'0090!,'0111!, '0112!,'0116!,'0117!,'0128! figures 2A,18,22,23,27	1-20
X	US 5 272 677 A (YAMAMURA RYUJI) 21 December 1993 (1993-12-21)	1,5
A	column 4, line 45 -column 5, line 32 column 5, line 60 - line 66 column 6, line 39 -column 7, line 31 figures 5,6	2-4,10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
10 May 2004	28/06/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Vertua, A

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/04519

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 01/53916 A (BROADCOM CORP ;LUTKEMEYER CHRISTIAN A J (US)) 26 July 2001 (2001-07-26) page 1, line 8-27 figure 1	1

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/04519

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2001054760 A1	27-12-2001	JP 2002083872 A	22-03-2002
		TW 488063 B	21-05-2002
US 5272677 A	21-12-1993	JP 3158542 B2	23-04-2001
		JP 5101679 A	23-04-1993
		KR 9605351 B1	24-04-1996
WO 0153916 A	26-07-2001	AU 3302301 A	31-07-2001
		EP 1250638 A2	23-10-2002
		WO 0153916 A2	26-07-2001
		US 2002093367 A1	18-07-2002
		US 2002089362 A1	11-07-2002
		US 2003038663 A1	27-02-2003
		US 2004025075 A1	05-02-2004
		US 2001049812 A1	06-12-2001
		US 2001030234 A1	18-10-2001

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Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 03/079172 A2

(54) Title: A POWER-DOWN SCHEME FOR AN ON-DIE VOLTAGE DIFFERENTIATOR DESIGN

(57) Abstract: According to one embodiment, an integrated circuit is disclosed. The integrated circuit includes a plurality of circuit blocks. Each circuit block includes a voltage differentiator that generates a local supply for the circuit block.

A POWER-DOWN SCHEME FOR AN ON-DIE VOLTAGE DIFFERENTIATOR DESIGN

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FIELD OF THE INVENTION

[0002] The present invention relates to integrated circuits; more particularly, the present invention relates to generating multiple power supply voltages on an integrated circuit.

BACKGROUND

[0003] Recently, power consumption has become an important concern for high performance computer systems. Consequently, low power designs have become significant for present-day very large scale integration (VLSI) systems. The most effective way to reduce power dissipation in an integrated circuit (IC) is by decreasing the power supply voltage (V_{CC}) at the IC.

[0004] In order to simultaneously achieve high performance and low power, multi-V_{CC} design, various techniques have been developed. However, due to the high cost of packaging and routing, it is typically difficult to generate multi-V_{CC} designs using traditional off-chip voltage regulators.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention. The drawings, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

[0006] **Figure 1** is a block diagram of one embodiment of an integrated circuit;

[0007] **Figure 2** is a block diagram of one embodiment of a circuit block; and

[0008] **Figure 3** illustrates one embodiment of a voltage differentiator.

DETAILED DESCRIPTION

[0009] A mechanism to power down one or more circuit blocks on an integrated circuit (IC) using on-die voltage differentiators is described. In the following description, numerous details are set forth. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

[0010] Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0011] **Figure 1** is a block diagram of one embodiment of an IC 100. According to one embodiment, IC 100 is partitioned into twenty-five circuit blocks 110. In a further embodiment, each circuit block 110 includes a voltage differentiator 120. Each voltage differentiator 120 generates a local power supply (V_{cc}_local) from an external power supply (V_{cc}_global). In one embodiment, differentiator 120 switches off V_{cc}_local whenever the particular circuit block 110 in which the differentiator 120 is included is operating in a standby state. One of ordinary skill in the art will appreciate that other quantities of circuit blocks 110 may be implemented within IC 100.

[0012] **Figure 2** is a block diagram of one embodiment of a circuit block 110. Circuit block 110 includes voltage differentiator 120, a functional unit block (FUB) 230 and a control module 250. FUB 230 is coupled to voltage differentiator 120. In one embodiment, FUB 230 is logic circuitry that may encompass various components within IC 100 (e.g., microprocessor logic, microcontroller logic, memory logic, etc.). FUB 230 is powered by V_{cc}_local received from voltage differentiator 120.

[0013] Control module 250 is coupled to voltage differentiator 120 and FUB 230. Control module determines the operation mode for circuit block 110 based upon the status of FUB 230 circuitry. According to one embodiment, control module 250 transmits a standby signal (SLP) to voltage differentiator 120. SLP is used to indicate whether FUB 230 is currently in an operating mode, or in a standby mode.

[0014] If FUB 230 is in an operating mode, control module 250 transmits a high logic level (e.g., logic 1) to voltage differentiator 120, indicating that V_{cc}_local is to be generated and forwarded to FUB 230. If, however, FUB 230 is idle,

control module 250 transmits a low logic level (e.g., logic 0) to voltage differentiator 120, indicating that FUB 230 is to be powered down. Thus, V_{CC}_local is not generated, and power is conserved.

[0015] **Figure 3** illustrates one embodiment of voltage differentiator 120. Voltage differentiator 120 includes resistors R1 and R2, a comparator 350, an inverter, a not-and (NAND) gate, a PMOS transistor (P) and a capacitor. Resistors R1 and R2 are used to generate a reference voltage (V_{REF}) for comparator 350. The reference voltage is specified by the equation $V_{REF} = R2^* V_{CC}/(R1 + R2)$. In one embodiment, V_{REF} may be tuned to a desired voltage at each circuit block 110 by changing the resistance values of resistors R1 and R2.

[0016] V_{REF} is received at one input of comparator 350. Comparator 350 receives a feedback of V_{CC}_local from transistor P at its second input. Comparator 350 compares V_{REF} to V_{CC}_local. If V_{CC}_local falls below V_{REF}, the output of comparator 350 is activated at logic 0. According to one embodiment, comparator 350 is an operational amplifier. However, one of ordinary skill in the art will recognize that other comparison logic circuitry may be used to implement comparator 350.

[0017] The inverter is coupled to the output of comparator 350 and inverts the output value received from comparator 350. The output of the inverter is coupled to one input of the NAND gate. The NAND gate receives the SLP signal at its second input. Whenever the output of the NAND gate and the SLP signal are both at logic 1, the NAND gate is activated to logic 0. In other embodiments, the inverter may not be included within voltage differentiator 120. In such embodiments, the NAND gate may be replaced with an and-gate.

[0018] The gate of transistor P is coupled to the output of the NAND gate. The source of transistor P is coupled to V_{CC}_global, while the drain is coupled to an input of comparator 350, the capacitor and FUB 230. Transistor P is activated whenever the NAND gate is activated to logic 0.

[0019] During the FUB 230 operating mode (e.g., SLP = logic 1), transistor P is activated whenever V_{CC}_local falls below V_{REF}. In particular, comparator 350 senses such a condition and is activated to logic 0. The inverter inverts the logic 0 signal into a logic 1. Thus, the NAND gate is activated to logic 0, activating the gate of transistor P. Transistor P charges the decouple capacitor, increasing V_{CC}_local. If V_{CC}_local is greater than V_{REF}, transistor P is turned off. Consequently, V_{CC}_local is always close to V_{REF}.

[0020] During the standby mode, the NAND gate is deactivated because of the received SLP value of logic 0. Accordingly, transistor P is turned off. V_{CC}_local will drop and leakage power attributed to circuit block 110 is significantly reduced.

[0021] The use of on-die voltage differentiators enables the generation of a local power supply voltage for each circuit block within an IC, which reduces the power dissipation. Moreover, the power down (or standby) control mechanism, combined with the on-die voltage differentiators drastically reduces leakage power during idle time for a circuit block.

[0022] Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is in no way intended to be considered limiting. Therefore, references to details of various embodiments

are not intended to limit the scope of the claims which in themselves recite only those features regarded as the invention.

CLAIMS

What is claimed is:

1. An integrated circuit comprising a plurality of circuit blocks, each circuit block having a voltage differentiator that generates a local power supply for the circuit block.

2. The integrated circuit of claim 1 wherein each of the plurality of circuit blocks operates in a normal power mode and a standby mode that enables the circuit blocks to switch off the local power supply.

3. The integrated circuit of claim 2 further comprising a first circuit block comprising:

a first voltage differentiator;

a first functional unit block (FUB) coupled to the first voltage differentiator; and

a first control module, coupled to the first voltage differentiator and the first FUB, that determines the operation mode for the first circuit block.

4. The integrated circuit of claim 3 wherein the control module generates a standby signal that is transmitted to the first voltage differentiator that indicates whether the first circuit block is to operate in the normal power mode or the standby mode.

5. The integrated circuit of claim 3 wherein the first voltage differentiator comprises:

a voltage reference generator that generates a reference voltage; and

a comparator, coupled to the voltage reference generator, that compares the reference voltage to the local power supply voltage.

6. The integrated circuit of claim 5 wherein the first voltage differentiator further comprises:

an inverter coupled to the output of the comparator;

a NAND gate having a first input coupled to the output of the inverter and a second input coupled to the control module for receiving the standby signal;

a PMOS transistor having a gate coupled to the output of the NAND gate and a drain coupled to the FUB and the comparator; and

a capacitor coupled to the drain of the PMOS transistor.

7. The integrated circuit of claim 5 wherein the comparator comprises an operational amplifier.

8. The integrated circuit of claim 5 wherein the voltage reference generator comprises:

a first resistor coupled to a global voltage power supply and the comparator; and

a second resistor coupled to the first resistor, the comparator and ground.

9. The integrated circuit of claim 3 further comprising a second circuit block, the second circuit block comprising:

a second voltage differentiator;

a second FUB coupled to the second voltage differentiator; and

a second control module, coupled to the second voltage differentiator and the second FUB, that determines the operation mode for the second circuit block.

10. A circuit block within an integrated circuit, the circuit block comprising:

a voltage differentiator that generates a local power supply for the circuit block;

a functional unit block (FUB) coupled to the first voltage differentiator; and

a first control module, coupled to the first voltage differentiator and the FUB, that determines whether the circuit block operates in a normal power mode and a standby mode that enables the circuit blocks to switch off the local power supply.

11. The circuit block of claim 10 wherein the control module generates a standby signal that is transmitted to the voltage differentiator that indicates whether the first circuit block is to operate in the normal power mode or the standby mode.

12. The integrated circuit of claim 10 wherein the voltage differentiator comprises:

a voltage reference generator that generates a reference voltage; and

a comparator, coupled to the voltage reference generator, that compares the reference voltage to the local power supply voltage.

13. The integrated circuit of claim 12 wherein the voltage differentiator further comprises:

an inverter coupled to the output of the comparator;

a NAND gate having a first input coupled to the output of the inverter and a second input coupled to the control module for receiving the standby signal;

a PMOS transistor having a gate coupled to the output of the NAND gate and a drain coupled to the FUB and the comparator; and

a capacitor coupled to the drain of the PMOS transistor.

14. The integrated circuit of claim 12 wherein the comparator comprises an operational amplifier.

15. The integrated circuit of claim 12 wherein the voltage reference generator comprises:

a first resistor coupled to a global voltage power supply and the comparator; and

a second resistor coupled to the first resistor, the comparator and ground.

16. A voltage differentiator comprising:

a voltage reference generator that generates a reference voltage from a global power supply; and

a comparator, coupled to the voltage reference generator, that compares the reference voltage to a local power supply voltage generated at the voltage differentiator.

17. The voltage differentiator of claim 16 wherein the voltage differentiator operates in a normal power mode and a standby mode that switches off the local power supply.

18. The integrated circuit of claim 16 wherein the voltage differentiator further comprises:

an inverter coupled to the output of the comparator;

a NAND gate having a first input coupled to the output of the inverter and a

second input coupled to a control module for receiving a standby signal;

a PMOS transistor having a gate coupled to the output of the NAND gate and a drain coupled to a functional unit block (FUB) and the comparator; and

a capacitor coupled to the drain of the PMOS transistor.

19. The integrated circuit of claim 16 wherein the comparator comprises an operational amplifier.

20. The integrated circuit of claim 16 wherein the voltage reference generator comprises:

a first resistor coupled to a global voltage power supply and the comparator; and

a second resistor coupled to the first resistor, the comparator and ground.

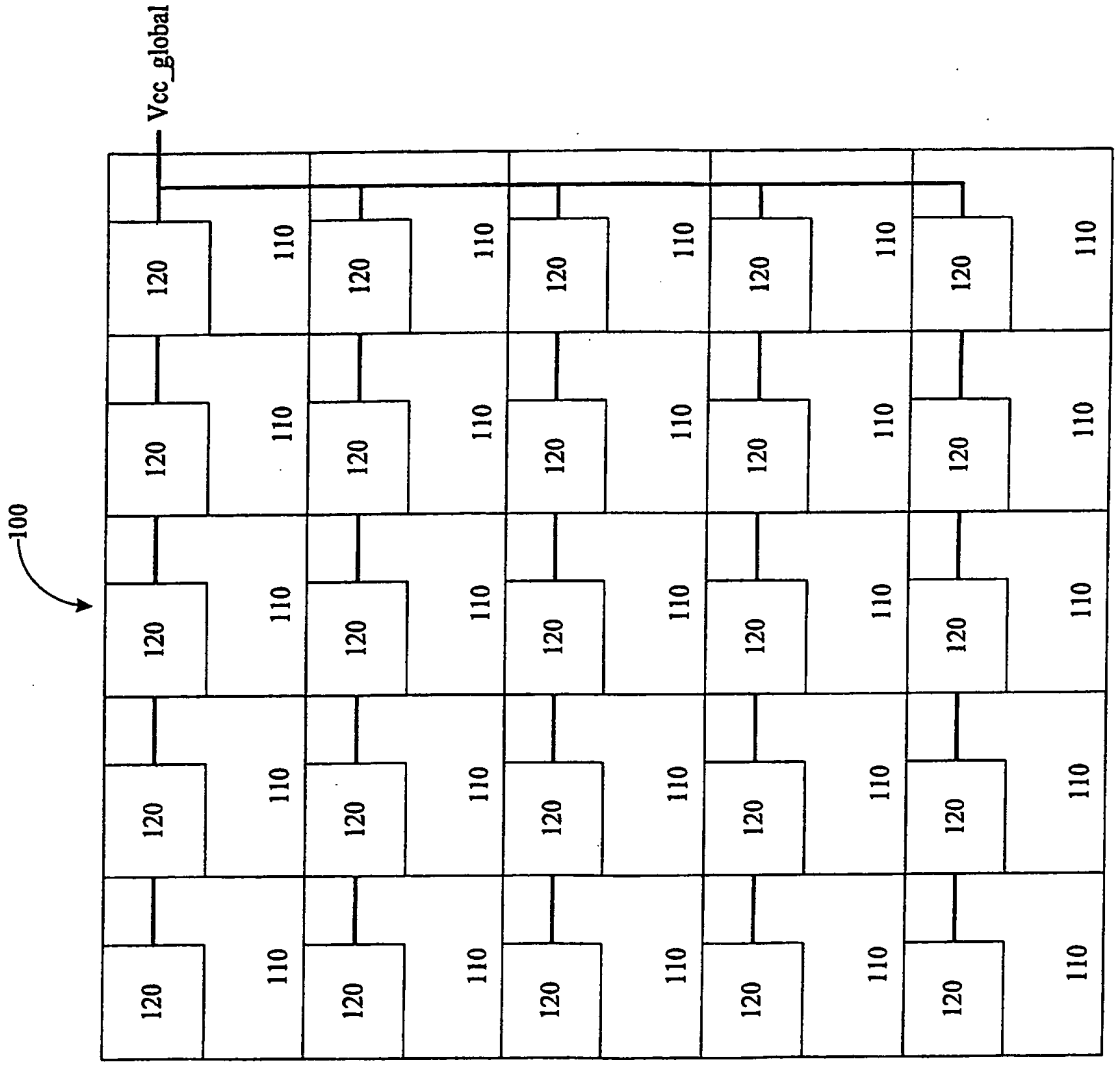

FIG. 1

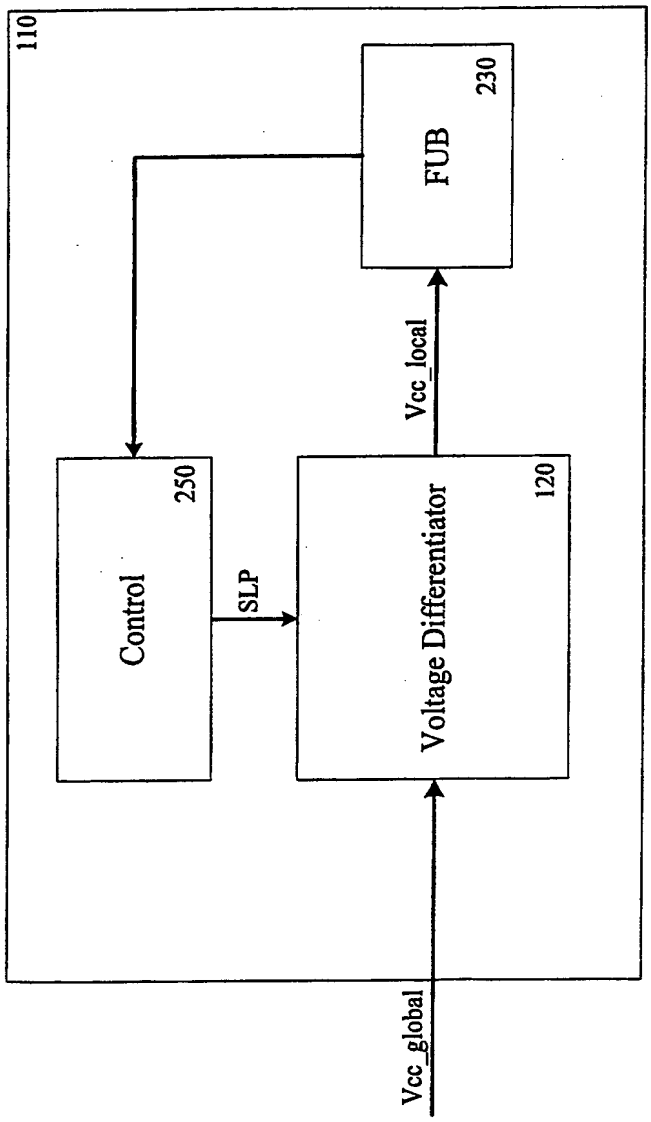
110
FUB
230
Vcc_local
Control
250
SLP
Voltage Differentiator
120
Vcc_global

FIG. 2

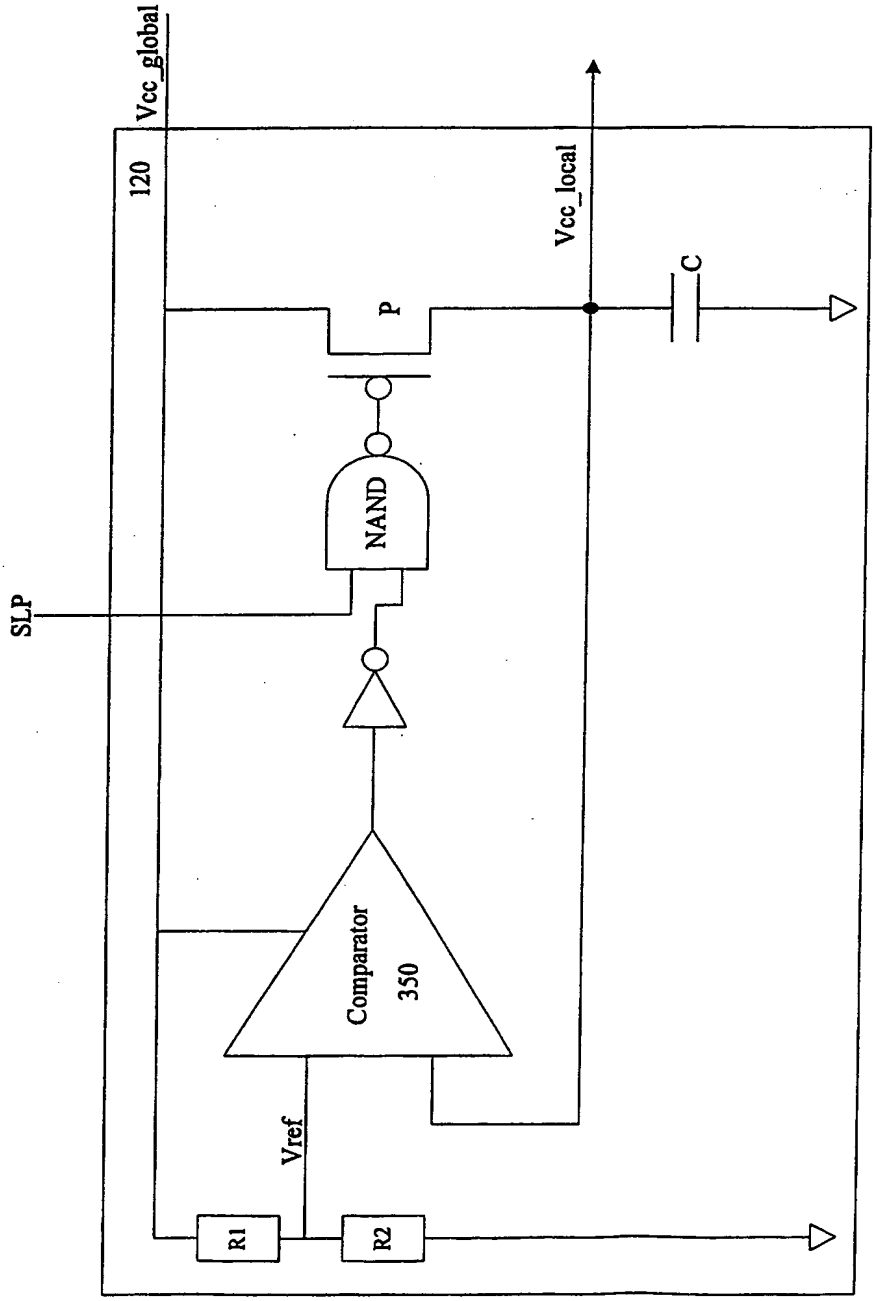
Vcc_global
120
Vcc_local
C
P
NAND
SLP
Comparator
350
Vref
R1
R2

FIG. 3